MAN1883

AMLC
User Guide

Revision 1
May 1974

PRIME
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HIGHLIGHTS OF AMLC

PRIME's AMLC is an efficient, flexible way to interface full-duplex asynchronous data lines to a PRIME computer. These lines can connect to RS232-C/CCITT V24 or 20 ma compatible terminals, peripheral devices, and 103/113/202 data sets. The AMLC performs bit-serial to/from character-parallel translation. A single circuit board services 8 or 16 lines. Additional boards are used to satisfy requirements for more than 16 lines.

Interfacing to the central processor is via programmed I/O, interrupt and direct memory transfer.

Flexibility is achieved by allowing software to select on a per line basis the speed, character format and parity. The AMLC has the capability to loop back each line and single-step the logic control clock. This helps isolate line and data set problems from the AMLC. Once failures have been isolated to a major unit or board, repair can be accomplished by simply replacing the board.

Transmission Type: Full or half duplex.

Interface to PRIME Computer:

Received data and/or line status	- DMA/ DMC
Transmitted data	- DMT
Line control and line configuration	- Programmed I/O
End of range for receive DMA/DMC channel	- Interrupt
Character time interval (if enabled)	- Interrupt
Data set control and status	- Programmed I/O
User-specified speed	- Programmed I/O

Software Controls (per line; enable/disable):

Transmit line break-space character
Transmit line mark character
Transmit data
Receive data
Receive off, report open line
Loop back
Echo mode
Interrupt every character time
Data set control

Status Reporting:

Open line (or break character)
Character overrun on received data
Incorrect stop bit
Data set status

Program Selectable Line Configuration Parameters:

Character size (exclusive of parity bit):

5, 6, 7 or 8 bits

Stop bits:

1 or 2 stop bits

Parity:

Odd, even or no parity; checked on incoming lines, generated on outgoing lines.

Echo:

On a character basis when enabled. Characters are received, checked, and retransmitted if correct.

Speed:

Under program control, each line can select one of eight clock speeds. Of these eight, four are fixed at 110, 134.5, 300 and 1200 baud. A fifth clock can be specified by the user. The clock is generated by the overflow from a preset 12 bit counter. The preset is implemented by a program loaded register. The remaining three clocks can be jumper selected by the user from the following speeds: 75, 150, 600, 1800, 2400, 4800, 9600, and 19,200 baud. Default selection is 75, 150, and 1800.

Data Set Interface (per line):

AMLC Type	Control	Status
5002, 5004	1) Request to Send 2) Data Terminal Ready 3) Originate Mode/Supervisory Transmit Data 4) Local Mode/Terminal Busy	1) Clear to Send 2) Data Set Ready 3) Carrier Detect 4) Supervisory Received Data
5052, 5054	1 control	1 status
5075	1 control *	1 status *

20 ma current loop lines (number 0-7) have no control/status lines

AMLC TYPE NUMBER DESCRIPTIONS

Type	Description
5002	AMLC for 103/113/202 data sets; RS232-C/CCITT V24, eight lines.
5004	AMLC for 103/113/202 data sets; RS232-C/CCITT V24, sixteen lines.
5052	AMLC for direct-connected devices: RS232/C/CCITT V24, eight lines
5054	AMLC for direct-connected devices: RS232-C/CCITT V24, sixteen lines.
5075	AMLC for direct-connected devices: eight lines @ 20 ma, plus eight lines @ RS232-C/CCITT V24.

5002, 5004 have full data set control: four control signals and four status signals per line.

5052, 5054 and 5075 have limited data set controls: one control signal and one status (or sense) signal per line. (5075: on RS232 lines only, not on 20 ma current loop lines).

PROGRAMMING

TABLE OF AMLC PIO INSTRUCTIONS

OP Code Bits 1-6	14_8	34_8	54_8	74_8
Function Code Bits 7-10	OCP	SKS	INA	OTA
00	Stop Clock		Input Data Set Status	Output Line # to Read DSS*
01	Single Step Clock			Output Line Configuration
02				Output Line Control
03				Output DSC*
04		Not Interrupting		
05				
06				
07			Input Status (& Clear)	
10				
11			Input I.D. Number	
12	Set Normal Mode			
13	Set Diagnostic Mode			
14			DMA/DMC Channel (RC)	DMA/DMC Channel (RC)
15	Set Int Mask		DMT Base Address (TX)	DMT Base Address (TX)
16	Clear Int Mask		Input Vector Address	Int Vector Address
17	Initialize			Programmable Asynch Clock

*on 5002, 5004 only

DEFINITION OF PIO INSTRUCTIONS

OCP'0000+DA	Stop AMLC System Clock. Used as debug aid and is effective only in the diagnostic mode.
OCP'0100+DA	Single Step AMLC System Clock. Used as debug aid and is effective only in the diagnostic mode.
OCP'1200+DA	Select Normal Mode of Operation. In this mode it is possible to run all lines and issue all OTA, INA commands.
OCP'1300+DA	Select Diagnostic Mode of Operation. In this mode it is possible to do all functions as in the normal plus OCP 'stop clock' and OCP 'single step clock' for debug purposes.
OCP'1500+DA	Set Interrupt Mask. Enables AMLC interrupts.
OCP'1600+DA	Clear Interrupt Mask. Disables AMLC interrupts.
OCP'1700+DA	Initialize AMLC. This command will clear all flip-flops and registers in the AMLC, start the AMLC clock and, over a period of one line scan, clear all the line control bits in RAMC to zero. For the period of the one line scan the AMLC will respond not ready to PIO instructions.
SKS'0400+DA	Skip if Not Interrupting. Tests AMLC Interrupt and skips if the AMLC is not interrupting.
INA'0000+DA	Input Data Set Status.
INA'0700+DA	Input AMLC Status.
INA'1100+DA	Input I.D. Number.
INA'1400+DA	Input DMA/DMC Channel Address.
INA'1500+DA	Input DMT Base Address.
INA'1600+DA	Input Vector Address
OTA'0000+DA*	Set up Line Number to Read Data Set Status.
OTA'0100+DA	Set up Line Configuration
OTA'0200+DA	Set up Line Control.

*On 5002, 5004 only

OTA'0300+DA* Output Data Set Control.

OTA'1400+DA Set up DMA/DMC Channel Address.

OTA'1500+DA Set up DMT Base Address.

OTA'1600+DA Set up Interrupt Vector Address.

OTA'1700+DA Set up Special Asynchronous Clock.

DA = Device Address. Standard DA = '54. In systems with multiple AMLC's, the DA can be changed by jumpers to uniquely identify each AMLC. INA and OTA instructions are more fully described in the "A-Register Format for OTA and INA Instructions" section below.

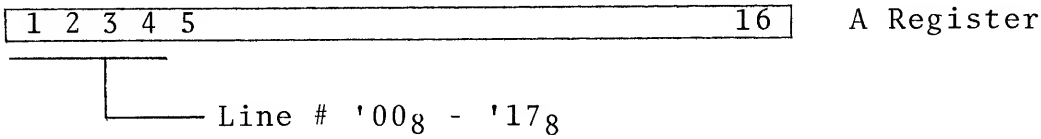
THE SKIP PROPERTIES OF THE OTA AND INA INSTRUCTIONS

INA'0700+DA, Input AMLC Status (and Clear), always skips. All other OTA and INA instructions will not skip if the AMLC common control logic is busy. Worst case delay is approximately 20 microseconds representing between .5% and 50% of the character time busy for 16 lines at 110 baud and 9600 baud, respectively. The "no-skip" condition should not be considered an error condition. The instruction will skip when the AMLC common control logic is not busy.

A REGISTER FORMAT FOR OTA AND INA INSTRUCTIONS

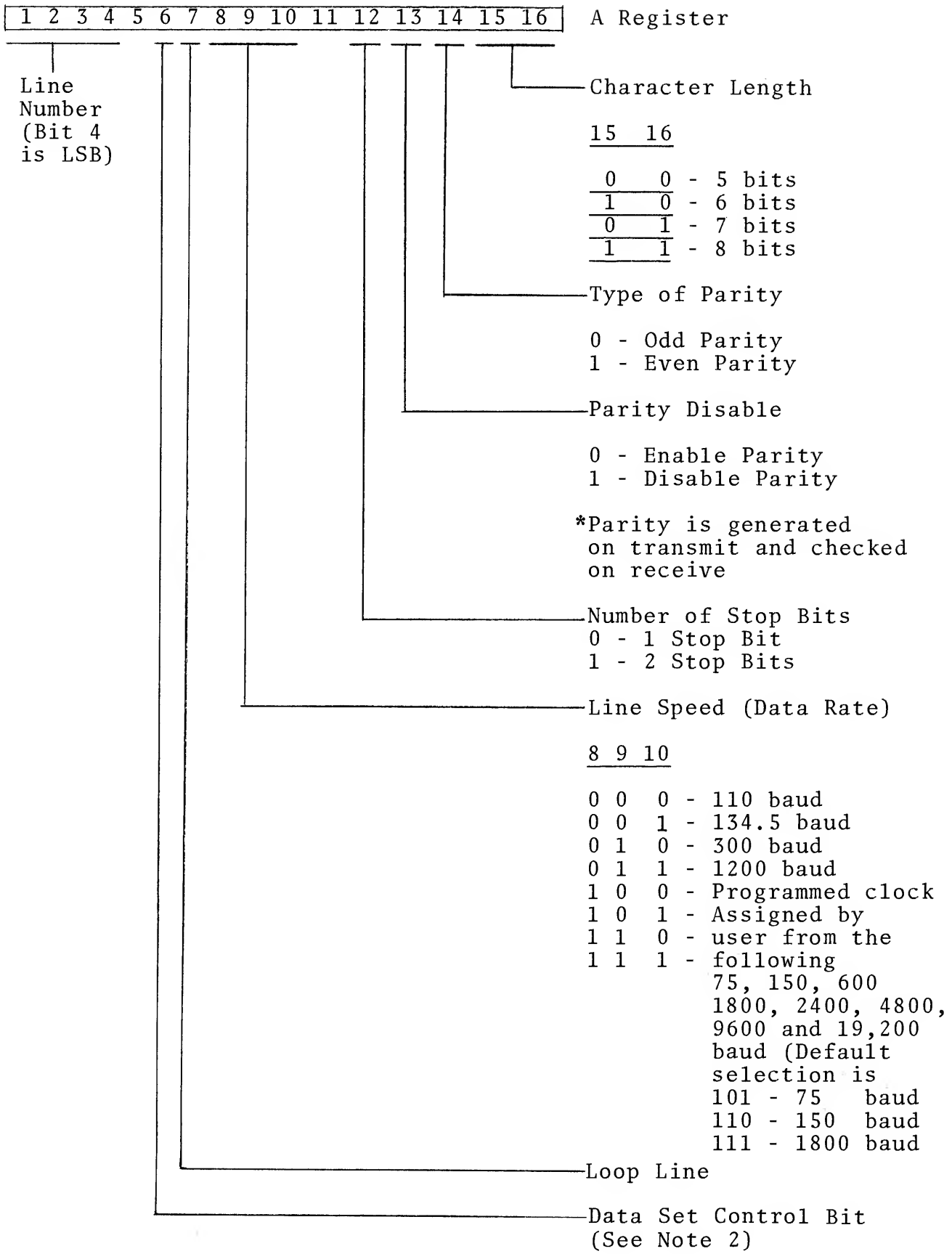
OTA'0000+DA (Model 5002, 5004 only) - Set up line number to read Data Set Status

Output Line number to read Data Set Status. This instruction should be followed immediately by INA'0000+DA (see below).



*On 5002, 5004 only

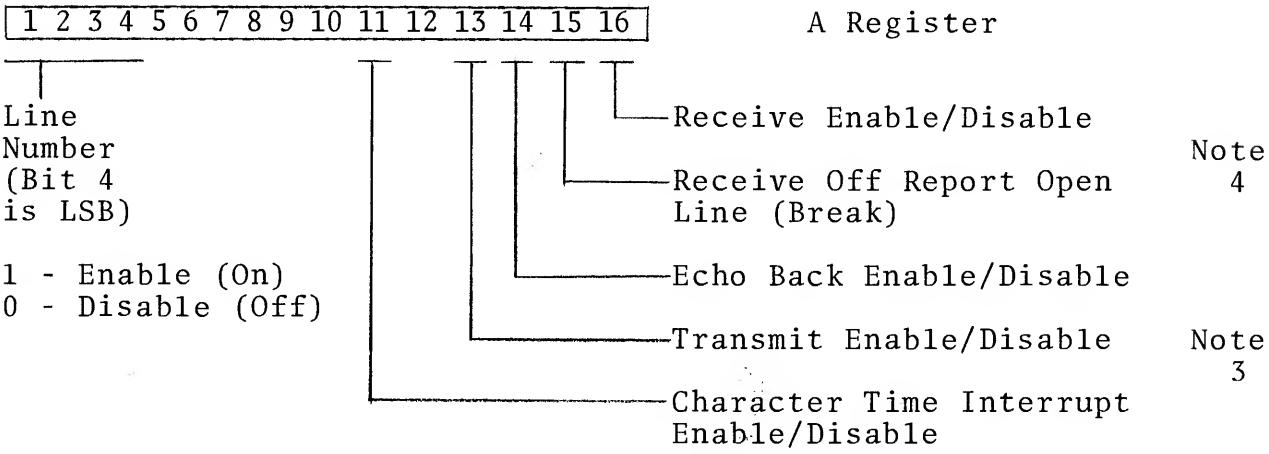
OTA'0100+DA - Set up line configuration



Note 1: The parity bit if enabled is additional to the character bits. (i.e. It is concatinated with the character. It is last bit to be transmitted.)

Note 2: On the basic AMLC board there is provided one control lead per line. Typically this could be used as "Request to Send" or "Data Terminal Ready" where some partial subset of full data set control is sufficient for customers uses. (Models 5052, 5054 only)

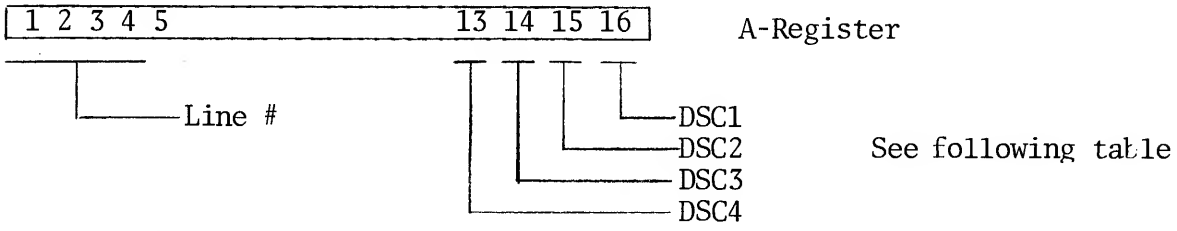
OTA'0200+DA - Set up line control



Note 3: Transmit and/or character time interrupts should not be enabled when echo back is enabled.

Note 4: Bits 15 & 16 should never both be set at any one time.

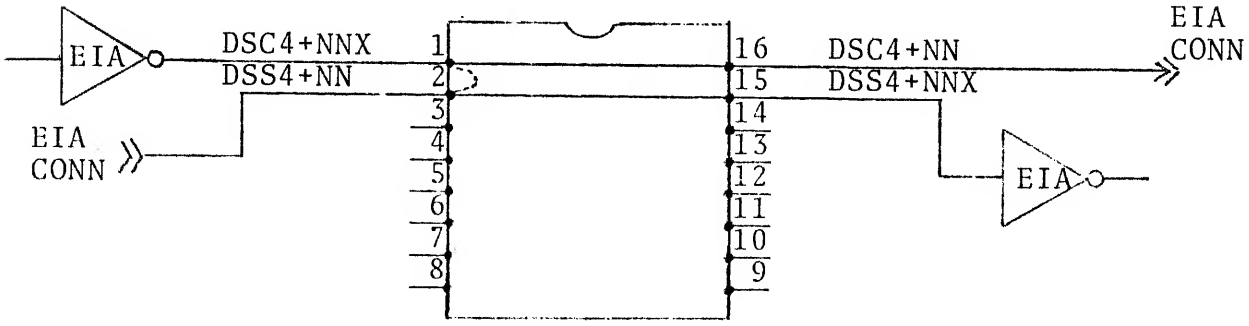
OTA'0300+DA - Output Data Set control (for 5002, 5004)



Data set control bit for types 5052, 5054 and the 8 EIA lines of the 5075 is set by OTA'0100+DA, Set up line configuration.

A Register Bit	SIGNAL/TYPE OF MODEM			
	103A	103F	202 C/D	113
16		Request to Send	Request to Send	
15	Data Terminal Ready		Data Terminal Ready	Data Terminal Ready
14		Originate Mode	Supervisory Transmit Data	
13		(Note 1) Local Mode		Terminal Busy

Note 1: Control of the 'Local Mode' lead on a type 103F modem can only be achieved by changing jumpers on the DSC board. See diagram below.

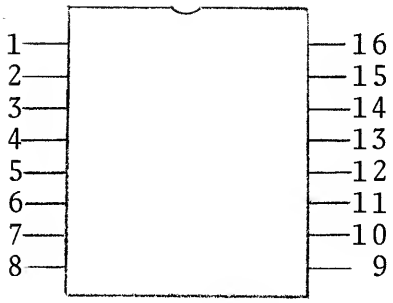


_____ normal jumpers

---------- jumper to enable control of "Local Mode"

There are four jumper DIP sites on the DSC at locations 6L, 14L, 29M and 43L. The jumper DIPs are set up as shown on the next page.

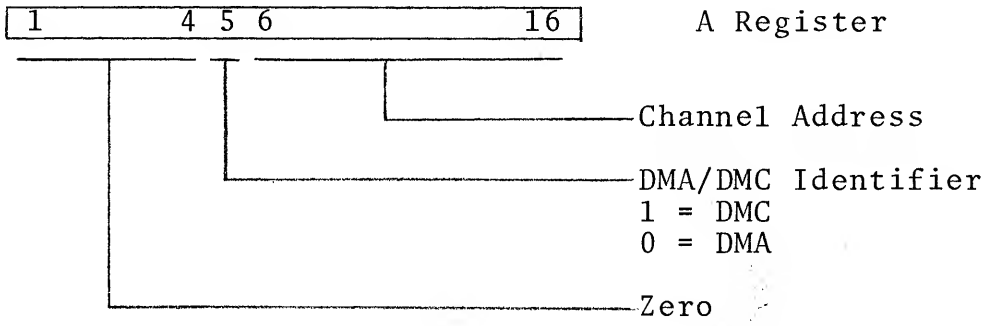
JUMPER/LINE ASSIGNMENT



DIPSITE/LINE #
JUMPER ASSIGNMENT

43L	29M	14L	6L
0	4	8	12
1	5	9	13
2	6	10	14
3	7	11	15

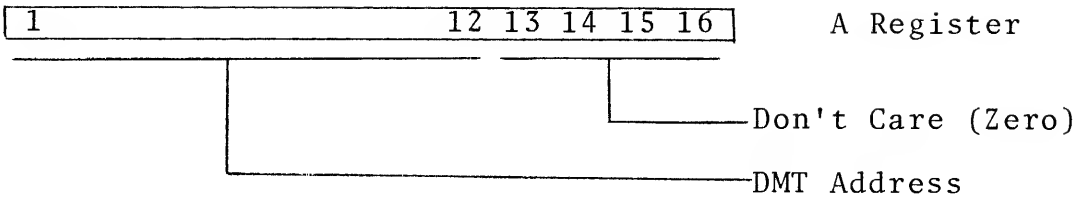
OTA'1400+DA - Set up DMA/DMC channel address



DMA/DMC channels are addressed by referencing the first word of the control word pair associated with each channel. DMA channel control word pairs are located in consecutive pairs of locations in the high speed register file (from location '20 through '37). The first pair of control words governs DMA channel one, the second pair governs channel two, and so on through locations '36 and '37 for channel eight. In each control word pair, the first word specifies the channel range (the two's complement of the number of words to be transferred: specified in bits 1-12) and the second word contains the address of the next word to be transferred. DMC control word pairs are located in consecutive pairs of main memory locations (from location '40 through '3776). In each DMC control word pair the first control word specifies the address of the next word to be transferred, and the second control word specifies the address of the last word to be transferred. All control words are set up under program control.

Further description of DMA/DMC operation is covered in the 'Format of Data in Memory" section on page 17.

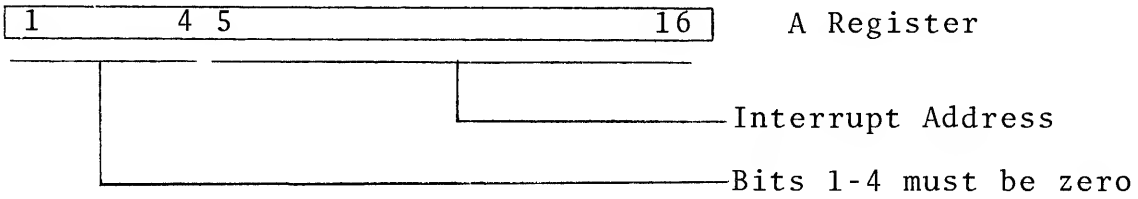
OTA'1500+DA - Set up DMT base address



The AMLC uses DMT to transfer data from memory for subsequent line transmission. In the DMT mode of operation, the AMLC provides the memory address of the data it requires. The base address is a pointer to the first word of an 8 or 16 word data stack; i.e., one word/line. The base address must have zeros in the 4 least-significant bits and be in the first 64K of memory. Each word or data cell is sequentially associated with a line on the AMLC. When the AMLC is ready to transmit a charactor on a line it adds the line number (0-17) with the base address and accessess the corresponding data cell. If the data cell contains a valid character, that character is transmitted and a second access to the data cell is made to clear it to all zeros. To output a string of characters, the program inspects the data stack for empty cells and fills them with the next character or line control. Due to the way DMT is used, no End Address is necessary. Address Bits 00 and 99 will always be zero.

Further description of DMT operation is covered in the 'Format of Data in Memory' section on page 15.

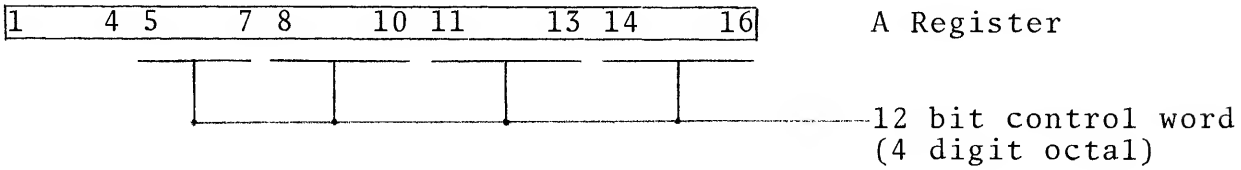
OTA'1600+DA - Set up interrupt vector address



The vector address is the memory address of the interrupt service routine. In the standard interrupt mode this address is always '63. In the vectored interrupt mode, a unique service routine can be written for each interrupt. The interrupt mode is selected by issuing either an ESIM (Enter Standard Interrupt Mode) or an EVIM (Enter Vectored Interrupt Mode) command.

There is a single interrupt associated with each AMLC controller. This interrupt represents selected Character Interval, End of Range (for DMA/DMC input transfers), or "Change of Data Set Status" (models 5002, 5004 only).

OTA'1700+DA - Set up special asynchronous clock

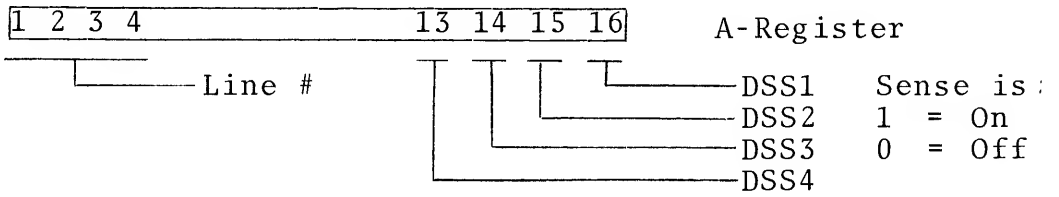


A 12 bit word is loaded into the A-register bits 5 through 16 and is output to a register on the AMLC which controls a 12 bit counter. Below is a table of constants to be loaded to generate certain specific data baud rates.

Baud Rate Required	Constant	Actual Baud Rate
30	'6557	30.001
45	'4777	45.002
50	'4377	50.002
55	'4056	54.991
100	'2177	100.005

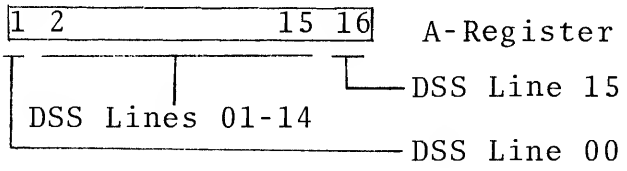
INA'0000+DA - Input Data Set Status

a) Type 5002, 5004: This instruction should follow an OTA '0000+DA



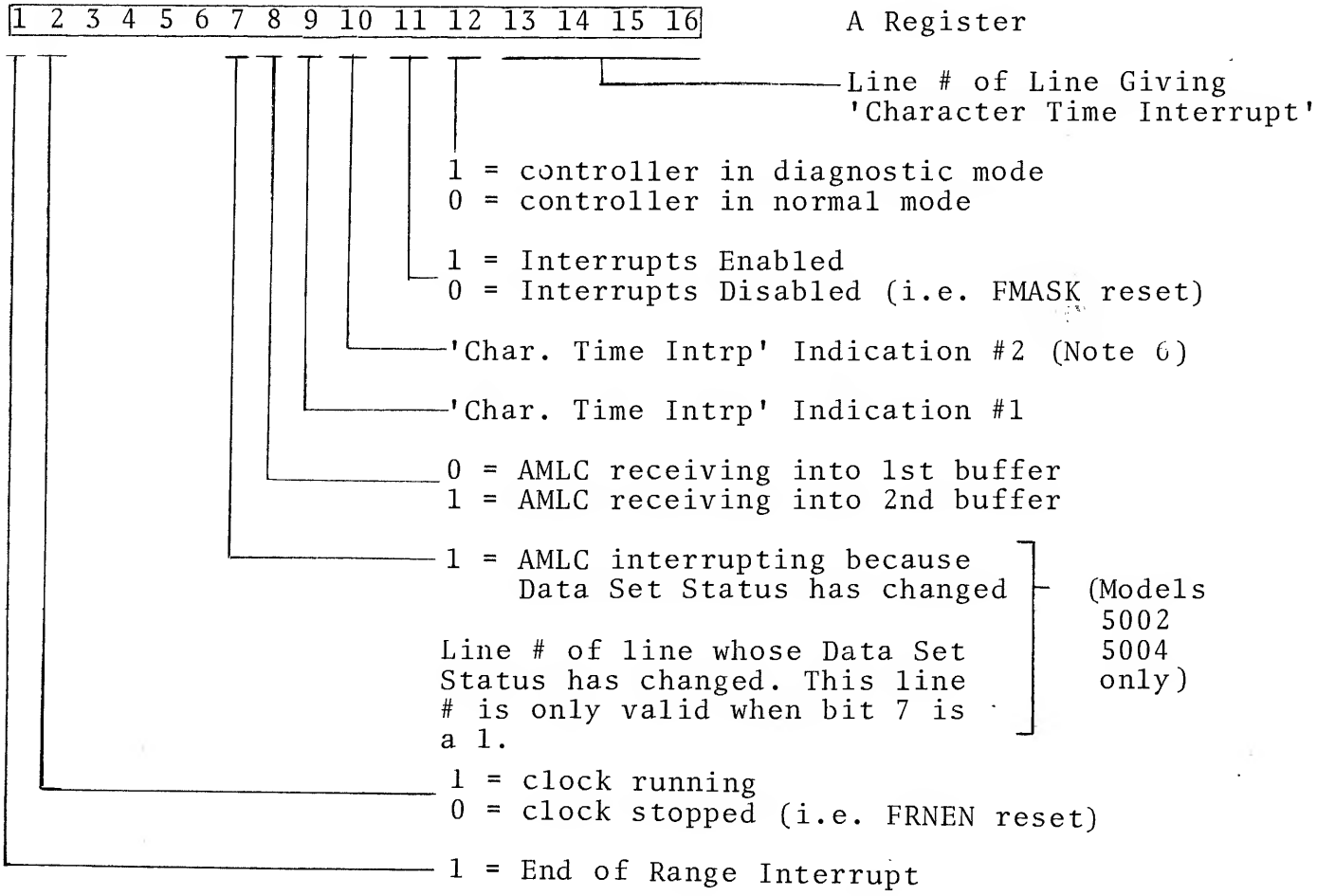
A Register Bit	SIGNAL/TYPE OF MODEM			
	103A	103F	202 C/D	113
16	Clear to Send	Clear to Send	Clear to Send	Clear to Send
15	Data Set Ready	Data Set Ready	Data Set Ready	Data Set Ready
14	Carrier Detect	Carrier Detect	Carrier Detect	Carrier Detect
13			Supervisory Received Data	

b) Type 5052, 5054, and 8 EIA lines of 5075:



Typically this bit will be used for 'Clear to Send' when connected to modems or peripherals with a serial EIA interface. Data sense in the A-Reg is: 1→Off, 0→On.

INA'0700+DA - Input AMLC status (and clear)

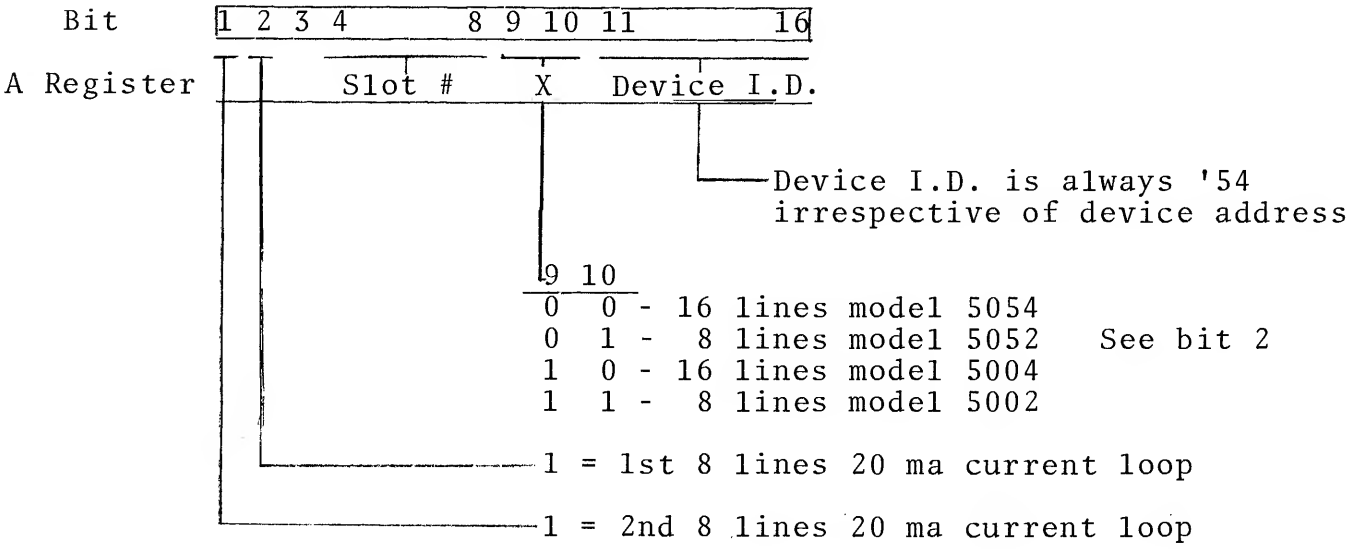


When INA '0700+DA is performed, bits 9, 10 and 13-16 are cleared to zero.

Note 6 - A character time interrupt will set bit 9 and put the line # on bits 13 through 16. If before an INA '0700+DA can be performed, a second character time interrupt occurs, bits 9 and 10 will both be set and a new line number will be set in bits 13 through 16.

Bits 9 and 10 both being set means that the line whose number is in bits 13 through 16 has interrupted and another line has previously interrupted but the line # has been overwritten.

INA'1100+DA - Input I.D. Number



The Slot # is encoded as follows:

Name	Conn Pin	I/O Bus Bit
BMCEXS1	A-87	4
BMCEXS2	A-89	5
BMCSS01	A-91	6
BMCSS01	A-93	7
BMCSS03	A-95	8

The Slot # is encoded on the backplane and this information is simply "passed on" during the INA. The X is for variation of the basic device type called out in the I.D. and is normally 00.

The Device I.D. is the standard device address for that type of device, in this case 54_8, and is intended to identify the type of device that is in the system.

In network applications, this instruction allows a common program to tailor itself for different configurations. It also permits the program to check if controllers have been placed in their proper slot after board replacement maintenance has been accomplished.

INA'1400+DA - Input DMA/DMC Channel Address

A-Register contents are identical to those shown for OTA'1400+DA.

INA'1500+DA

A-Register contents are identical to those shown for OTA'1500+DA.

INA'1600+DA

A-Register contents are identical to those shown for OTA'1600+DA.

Format of Data in Memory

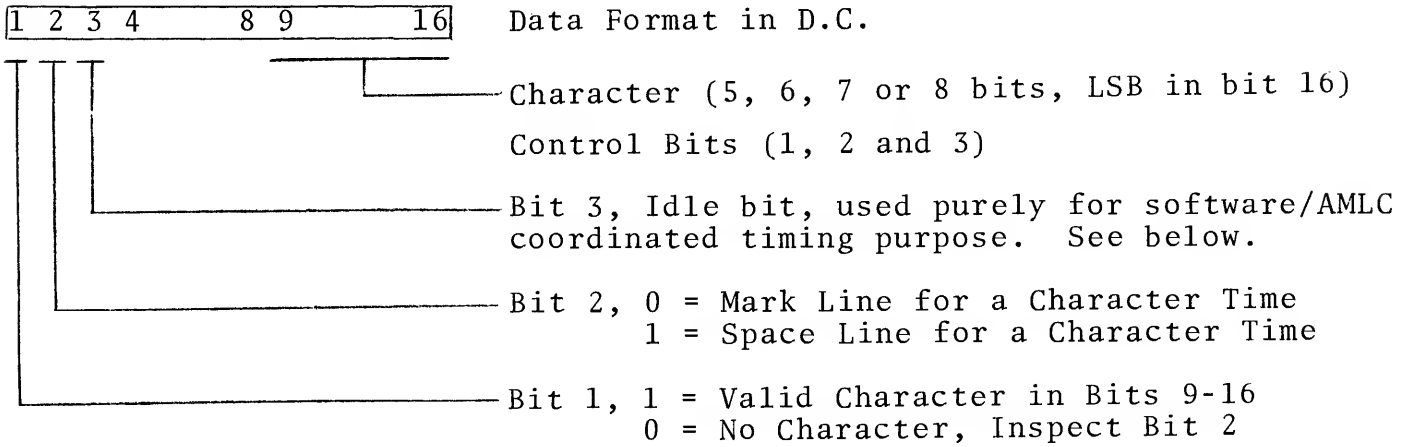
Data transfers between CPU and AMLC are by DMA or DMC for 'Received Data' and 'Line Status' (i.e. frame error, break, etc.) and DMT for Transmit Data.

Transmit Data

A location in RIORF will store bits 1-12 of the DMT address and bits 00 and 99 will always be zero.

This 14 bit address will locate a CPU memory address the last four bits of address being zero. By concatenating the four bit line number with the stored 14 bit address and presenting the whole 18 bits on the address lines during DMT cycles the AMLC can accrss a block of 16 CPU memory cells anywhere in 64K of memory. These 16 cells will be referred to as dedicated cells.

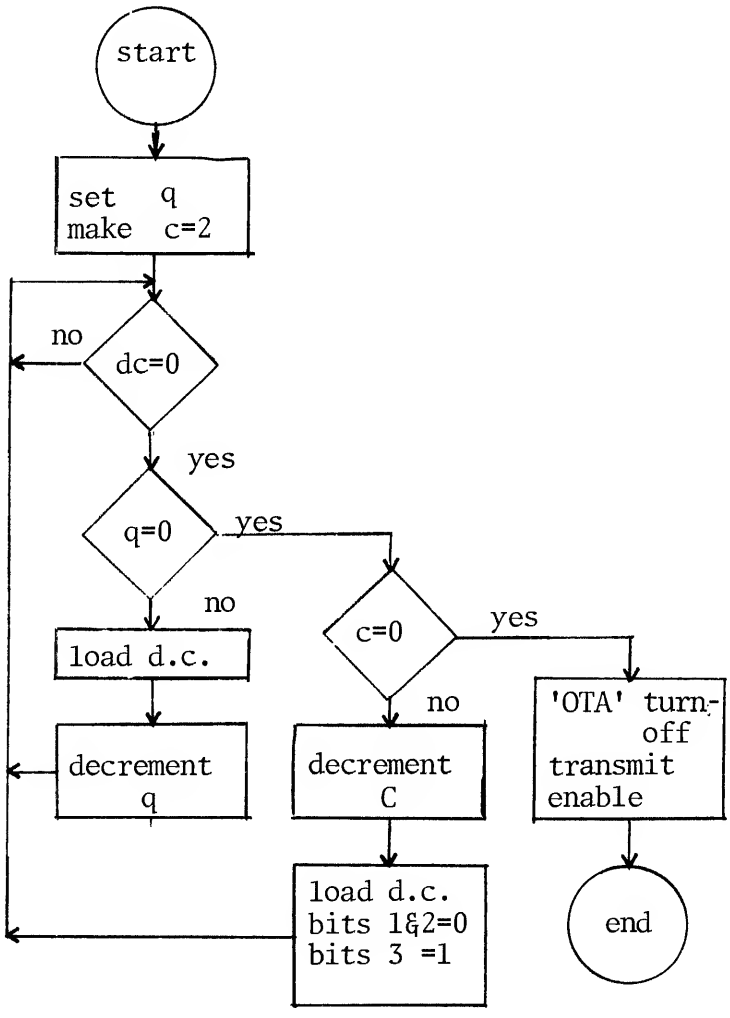
When a DMT request is made the AMLC will fetch the contents of the dedicated cell (D.C.) and inspect bits 1, 2 and 3, the data format is shown below.



The AMLC will input the DC to the RD register and will inspect bits 1, 2 and 3. If any of these bits is a 1 the AMLC requests another DMT cycle, but this time make an input with an all zero character to clear DC. The software knows when it sees DC cleared that data has been taken.

Within the AMLC bits 1 and 2 are always transferred with the character field to the line interface. Bit 3 is used as a timing device as follows:

The use of UARTs in the line interface means that from the time the last character in a message is taken from the DC, approximately two character times will elapse before it is safe to disable transmit and enable receive. Let us assume that the software will maintain a queue (q) to indicate the number of characters left in a message and provide two bits per line as a two bit counter (C). To turn a line off at the end of a message bit 3 is set each time the DC is filled and used as an indication to software that the DC has been fetched by the AMLC. Bits 1 and 2 being zero means the line will start to mark at the conclusion of the message. The flow chart below explains the sequence of events to be followed.



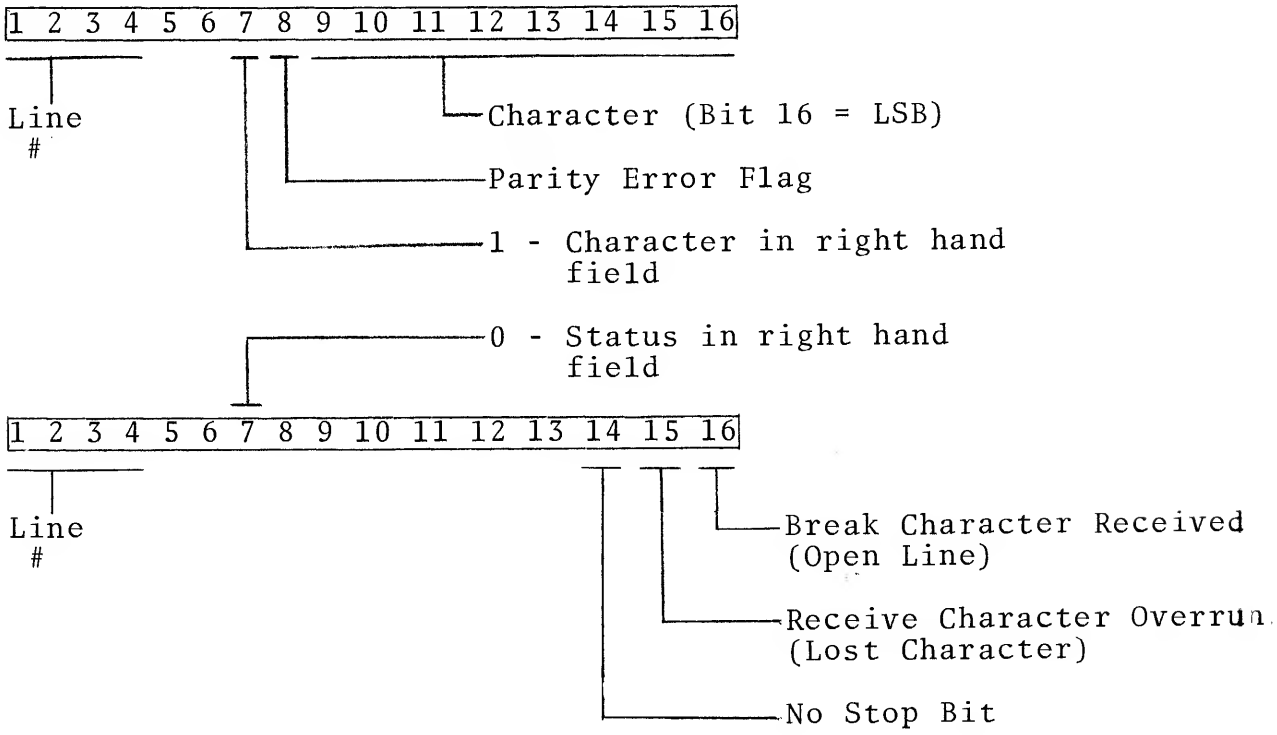
Receive Data and Line Status

Received data and line status is inputted to the CPU via DMA or DMC. Input is to a tumble table, i.e. each input contains a line number and data and causes the DMA/DMC base address to increment.

Although only one DMA or DMC channel address is output to the AMLC OTA'1400+DA, two adjacent channels will be used, i.e. two buffers in CPU memory. Bit 15 of the channel address is toggled by the AMLC every time an End of Range occurs. Thus, an End of Range will not cause loss of data if the software inputs AMLC status (INA'0700+DA within a buffer time.

Bit 8 of the AMLC status word will define which of the two input buffers the AMLC is currently using.

Format for Received Data



Start up Procedure Operation	Instruction
1. Identify all AMLCs in system	INA'11XX
2. Initialize controller and clear all line control flags in RAMC (i.e. TX enable, RC enable, etc).	OCP'1754
3. Set up transmit DMT channel i.e.,output base address of block of 16 decidated cells for transmit characters.	OTA'1554
4. Set up 2 receive DMA/DMC channels in CPU.	See CPU Reference Manual
5. Output receive DMA/C address to AMLC.	OTA'1454
5a. Set up vector address in CPU.	
6. Output interrupt vector address to AMLC	OTA'1654
7. Set interrupt mask	OCP'1554
8. Output constant per programmable baud rate clock.	OTA'1754
9. At this point if the AMLC configuration is known, all lines can be configured by an OTA'0154 and later, when one wishes to transmit, receive,an OTA'0254. or if polling terminals which are not all the same speed or data format, the OTA'0154 (configuration) may be performed just prior to the OTA'0254 (transmit enable, receive enable, etc.). Either way OTA'0154 always precedes OTA'0254.	

Note: MASTER CLEAR (HSYSCLR) condition, stops the AMLC clock, clears the UART, MARKS all lines. Start-up procedure should follow a MASTER CLEAR condition.

Continuation Procedures

These can vary from system to system but the flow chart in Figure 1 will give a general picture.

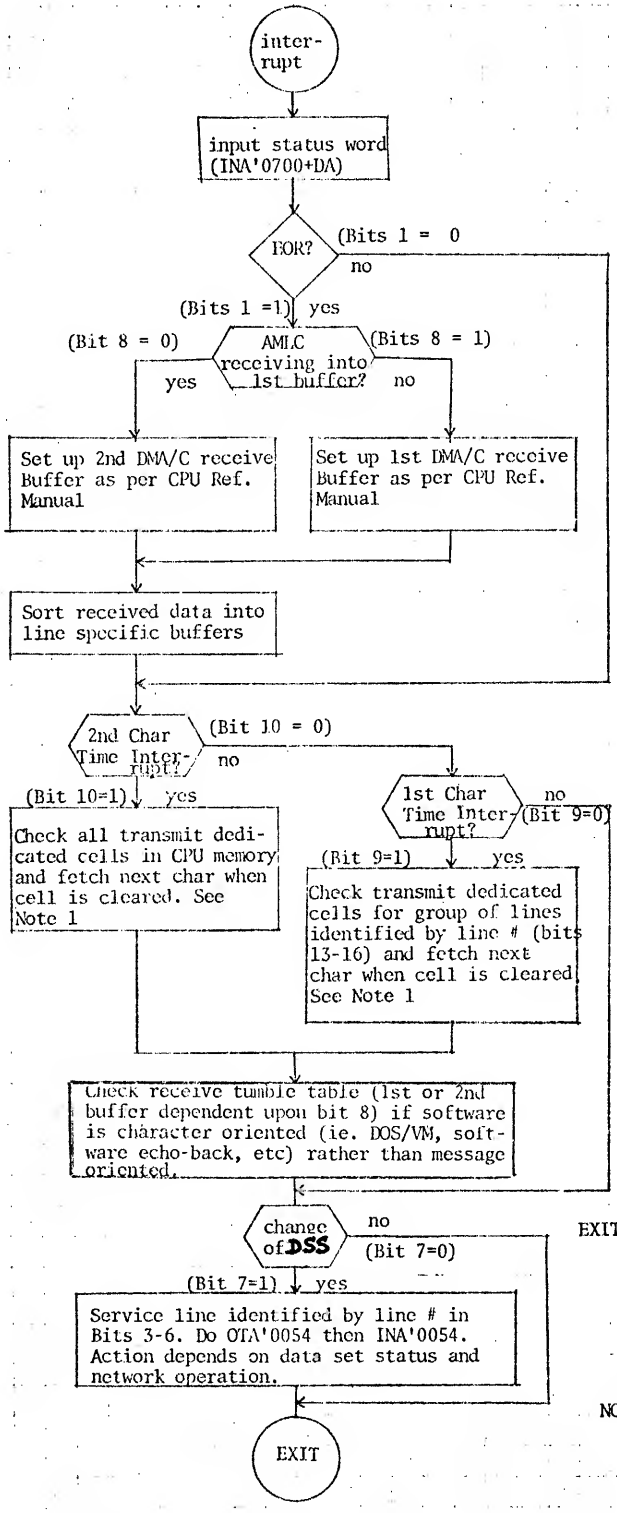


Figure 1

NOTE: When fetching next character a pointer must be incremented for each line. If there is no next character the line may be turned off (i.e. transmit disable with OTA'0254) or allowed to idle with dedicated cell empty.

Interrupts

End of Range (EOR)

The End of Range flip-flop (DEORF) is set by a signal from the CPU when one of the allocated DMA/DMC blocks of CPU memory has been filled. DEORF being set will cause the AMLC to change the channel address to the alternate buffer.

The interrupt routine should include an INA'0700+DA and the EOR will show up as bit 1 in the A-Register being set. INA'0700+DA will also clear the EOR.

Character Time Interrupts

Each line has a control bit enabling it to generate an interrupt every time the Transmit Buffer is empty. This interrupt will work regardless of the state of Transmit Enable, but should not be enabled when echo back is enabled.

When the software enters the AMLC interrupt routine it should perform an INA'0700+DA. Bit 9 is the 'Character Time Interrupt' indication and bits 13-16 comprise the line number of the line causing the interrupt. The INA'0700+DA will reset bits 9 and 13-16 to zero.

This feature can remove the need for a Real Time Clock option.

Shut-Down Procedures

There is no specific shut down procedure. Some systems may leave Receive enabled all the time and rely on software recognition of a specific character where initiation of communication is from an outside source.

Other systems would always shut down Transmit Enable/Receive Enable when communications with the line is not required.

General Block Diagram Description

The main component parts of the AMLC Block Diagram are:

a) RIORF

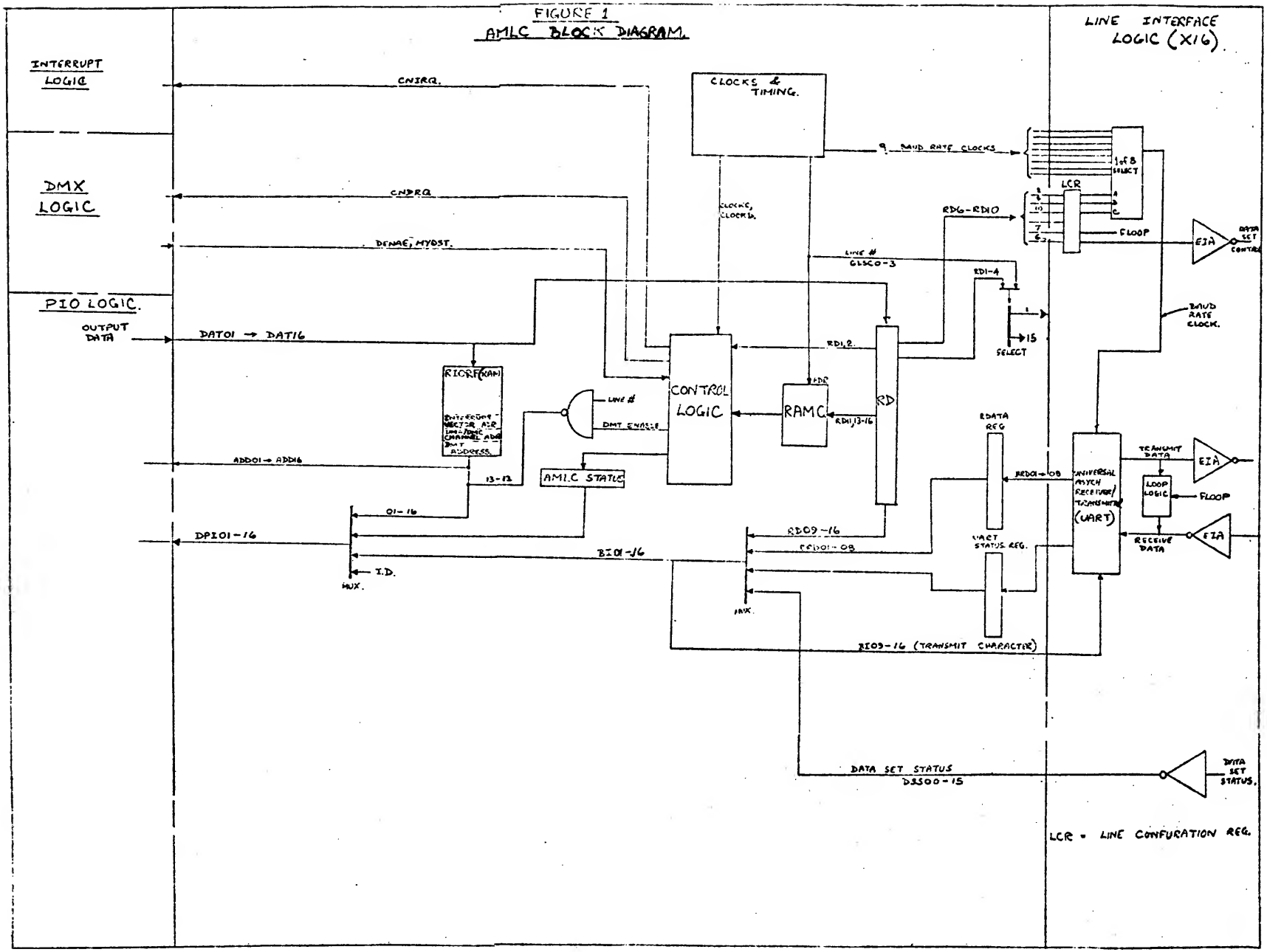
This is a 16 X 16 RAM used as registers for the:

1) Interrupt Vector Address

2) DMA/DMC Channel Address

3) DMT Address (Bits 13-16 come from line number).

FIGURE 1
AMLC BLOCK DIAGRAM.



b) AMLC Status Register

This is a combination of registers and individual flip flops which can be interrogated by an INA'0700+DA to ascertain AMLC status.

c) RAMC

This is an 8 X 16 RAM. One memory location is allocated per line for the following control bits:

1) Transmit Enable

2) Receive Enable

3) Receive Off Report Open Line

4) Echo Mode

5) Enable Character Time Interrupts

d) RD Register

This is a 16 bit register. It is used as temporary storage of 1) transmit character from CPU before they are transferred to the *UART in the line logic, 2) line control bits to be written into RAMC and 3) line configuration bits to be transferred to the UART.

e) Clocks and Timing Logic

This logic includes a crystal oscillator and various counters to produce:

1) A line scan RLSCO-3 ORed with RD1-4 to produce GLSCO-3.

2) Timing and clocks for the control logic (clock A, clock C, etc.).

3) 13 baud rate clocks of which eight will be used by the AMLC in any one configuration.

f) Line Interface Logic

This logic consists of 16 UARTs and associated logic to enable transmission of mark or space characters, select one of eight clocks, and loop the transmit data to the receive input. Also included are one data set control bit and one data set sense bit per line.

*UART = Universal Asynchronous Receiver/Transmitter

g) Control Logic

This logic takes the outputs of the UART Status Register and the control bits from RAMC and decides what action to take, i.e., DMT request for next transmit character, DMT input to clear CPU dedicated cell is a valid character received from CPU, or DMA/DMC inptu to CPU with a received character at line status condition. This logic also writes new configuration and line control words when the I/O flag (FIOBY) is set.

h) UART Status Register

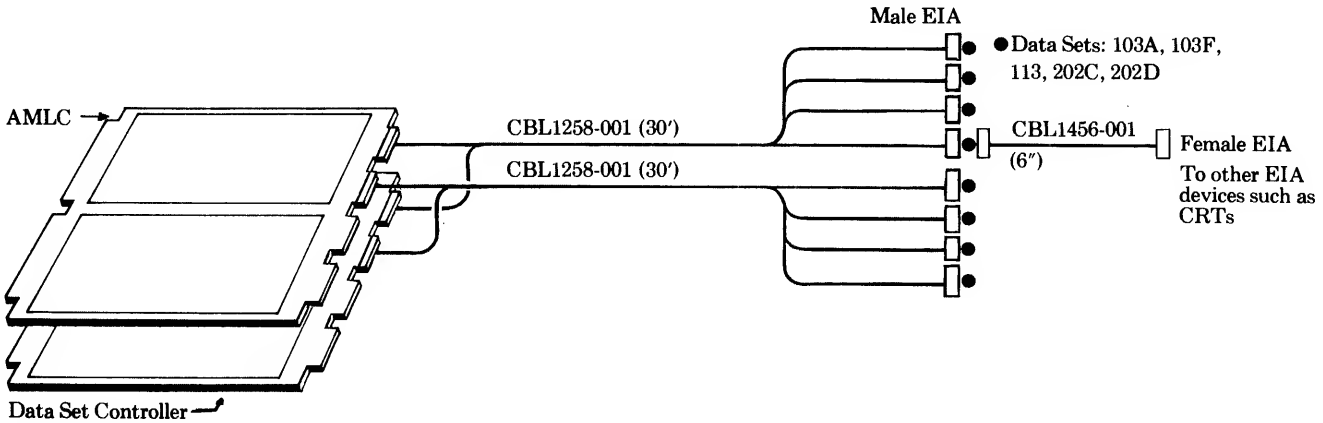
This is a 6-bit register used to hold UART status for use by the control logic. Bits shored are: Receive Data Available; Receive Data Parity Error; Receive Data Framing Error, Overrun Flag; Transmit Buffer Empty.

i) Received Data Register

Used to store Received Data from UART.

How to Order

Asynchronous multiline controller (AMLC) for type 103/202 data sets



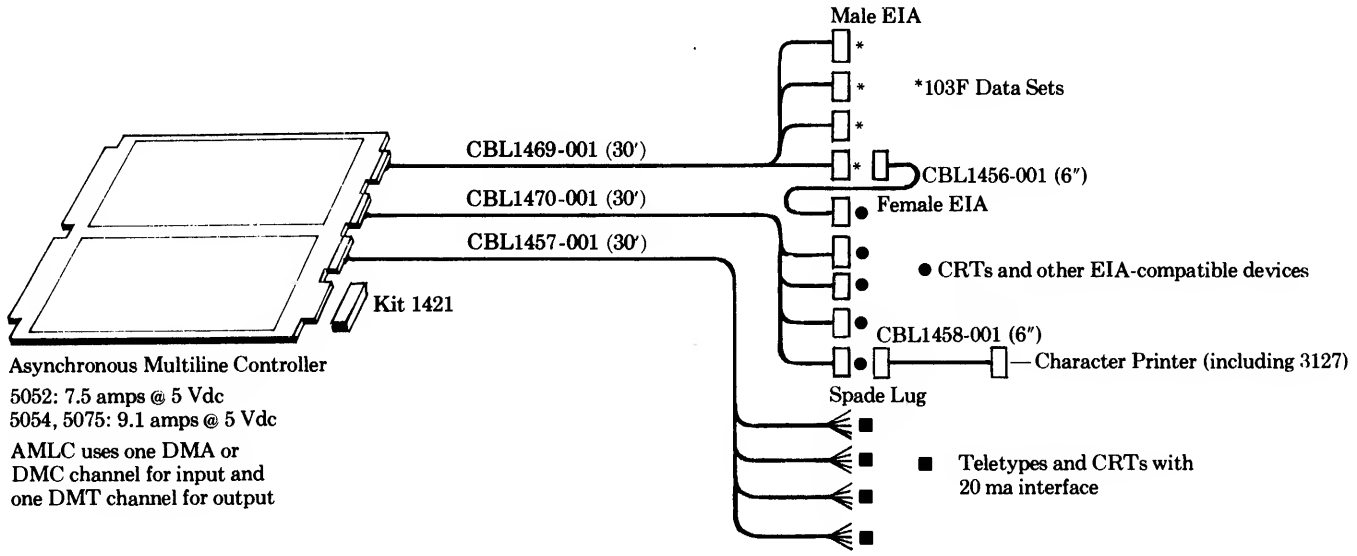
5002: 8.6 amps @ 5 Vdc
5004: 11.0 amps @ 5 Vdc

Each AMLC/Data Set Controller combination uses one DMA or DMC channel for input and a DMT channel for output.

Type	Description	Prerequisite
5002	AMLC for 103/202 data sets: RS232-C/CCITT V24, eight lines.	Any Prime CPU with DMC/DMT
5004	AMLC for 103/202 data sets: RS232-C/CCITT V24, 16 lines.	Any Prime CPU with DMC/DMT
CBL1258-001	Cable from AMLC and data set controller to four male EIA connectors (30′).	None
CBL1456-001	Cable adapter: male EIA to female EIA (6″).	None

Notes:
Cables are not included in the price of the AMLC and must be ordered separately.
When CRTs (3129) are purchased from Prime for use with the AMLC (5002 or 5004), an adapter cable (CBL1456-001) will be included with each CRT.
See page 20 for cable signal/connector pin list.

Asynchronous multiline controllers (AMLC) for direct-connected devices



Type	Description	Prerequisite
5052	AMLC for direct-connected devices: RS232-C/CCITT V24, eight lines.	Any Prime CPU with DMC/DMT
5054	AMLC for direct-connected devices: RS232-C/CCITT V24, 16 lines.	Any Prime CPU with DMC/DMT
5075	AMLC for direct-connected devices: eight lines @ 20 ma, plus eight lines @ RS232-C/CCITT V24.	Any Prime CPU with DMC/DMT
CBL1469-001	Cable from AMLC to four male EIA connectors (30′).	None
CBL1470-001	Cable from AMLC to four female EIA connectors (30′).	None
CBL1457-001	Cable from AMLC to four 4-wire spade lug terminations (30′).	None
CBL1456-001	Cable adapter from male EIA to female EIA (6″).	None
CBL1458-001	Cable adapter from female EIA to character printer (6″).	None
Kit 1421	Rear edge connector kit with pins and mtg. hdwr.	None

Notes:

Cables and connector kits are not included in the price of the AMLC and must be ordered separately.

CRTs (3129) purchased from Prime for use with AMLC are provided with cable CBL1470-001 (one cable per four CRTs).

Teletypes (3101-3105) purchased from Prime for use with AMLC are provided with cable CBL1457-001 (one cable per four Teletypes).

Character printer (3127) purchased from Prime for use with AMLC is provided with adapter cable CBL1458-001.

See page 20 for cable signal/connector pin list.

Cable signal/connector pin list for serial devices and data sets

	PORT #1 (J1)						PORT #2 (J2)						PORT #3 (J3)						PORT #4 (J4)					
	Transmit	Receive	Control	Status	Ground	Jumper	Transmit	Receive	Control	Status	Ground	Jumper	Transmit	Receive	Control	Status	Ground	Jumper	Transmit	Receive	Control	Status	Ground	Jumper
CBL1449-001	3	2	4	5	7		3	2	9	11	7	[6 8 20]	3	2	9	[4 5 8 20]	7		3	2	9	[4 5 6 20]	7	
CBL1224-001	3	2				[7 1] [4 5 8 20]	3	2				[7 1] [4 5 8 20]	3	2				[7 1] [4 5 8 20]	3	2				[7 1] [4 5 8 20]
CBL1430-001	√	√																						
CBL1453-001	√	√																						
CBL1297-001	√	√					√	√					√	√					√	√				
* CBL1457-001	√	√					√	√					√	√					√	√				

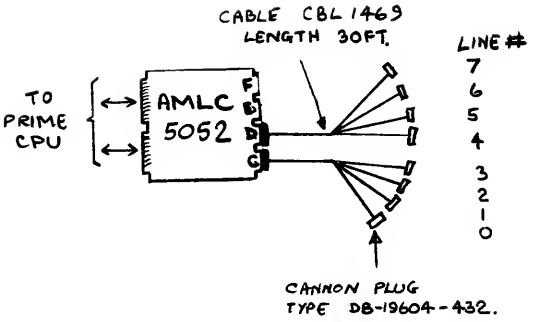
√ = Lug termination, signal & ground pair.

	Transmit Data	Receive Data	Request to Send	Clear to Send	Data Set Ready	Signal Ground	Data Carrier Detect	Transmit Clock	Receive Clock	Data Terminal Ready	Signal Quality Detect	Speed Select	Supervisory Trans. Data	Supervisory Rec. Data	Terminal Busy	Spare	Send New Sync.	
	F	T	F	T	T		T	T	T	F	T	F	F	T	F	F	F	T = to, F = from CPU
* CBL1258-001 J1-J4	2	3	4	5	6	7	8			20			[11 14]	[12 16]	25			C = Control S = Status
* CBL1469-001 J1-J4	2	3	4C	5 S		7												
* CBL1470-001 J1-J4	3	2	[4 5]	[4 5]		7	[8 20] S			[8 20]	S					9 C		
CBL1471-001 J1, J2	2	3	4	5	6	7	8	15	17	20	21	23						
CBL1472-001 J1, J2	2	3	4	5	6	7	8	15	17	20								
* CBL1456-001	3	2	[4 5]	[4 5]		7	[8 20]			[8 20]						9		Adapts CBL1469-001 to CBL1470-001
* CBL1458-001	3	2			[6 8 20]	7	[6 8 20]			[6 8 20]				11		9		Adapts CBL1470-001 to character printer (3127)

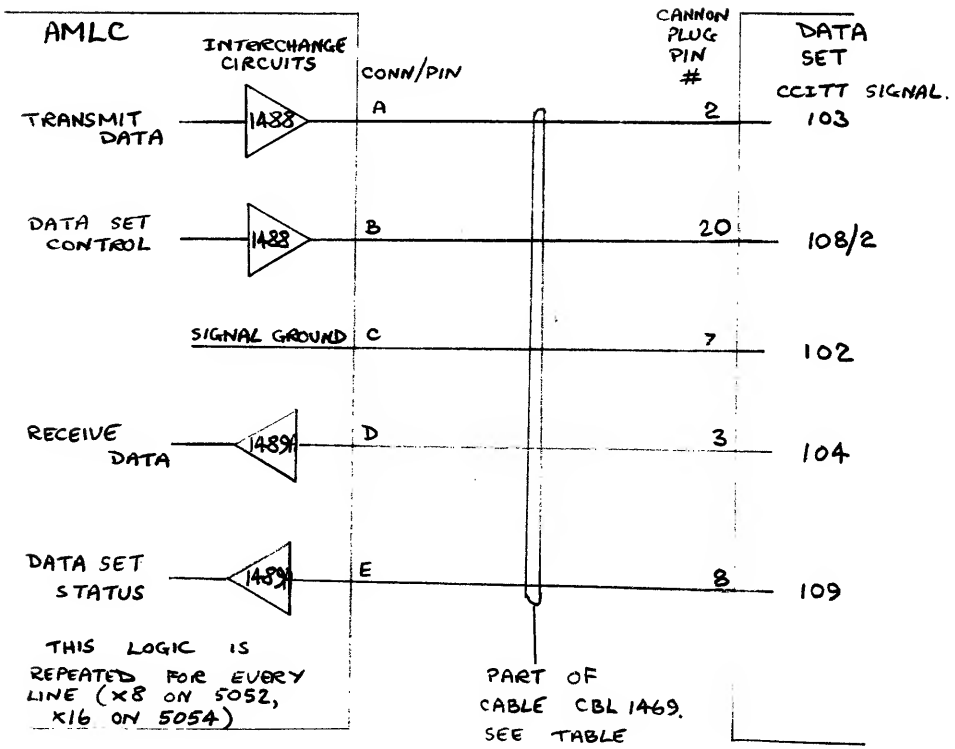
The table above summarizes cable signal/connector pin assignments for standard cables between communication controllers and serial I/O devices and data sets. All connectors, except lug terminations, are EIA-compatible. Use this table to determine if cable modifications are necessary to handle specific user devices.

*for use with AMLC

FIG 2 MODEL 5052, 5054 AMLC WITH CABLE "CBL 1469"



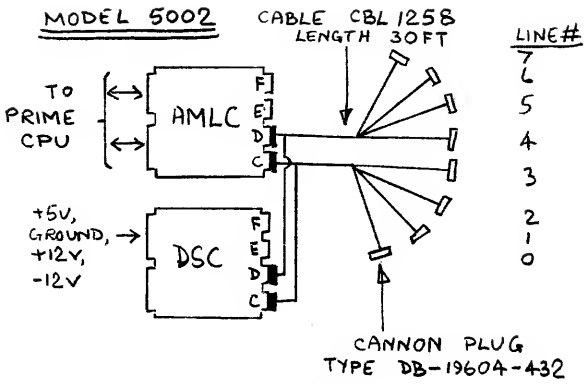
NOTE 1: MODEL 5054 IS IDENTICAL EXCEPT IT REQUIRES FOUR CABLES TO SERVICE SIXTEEN LINES.



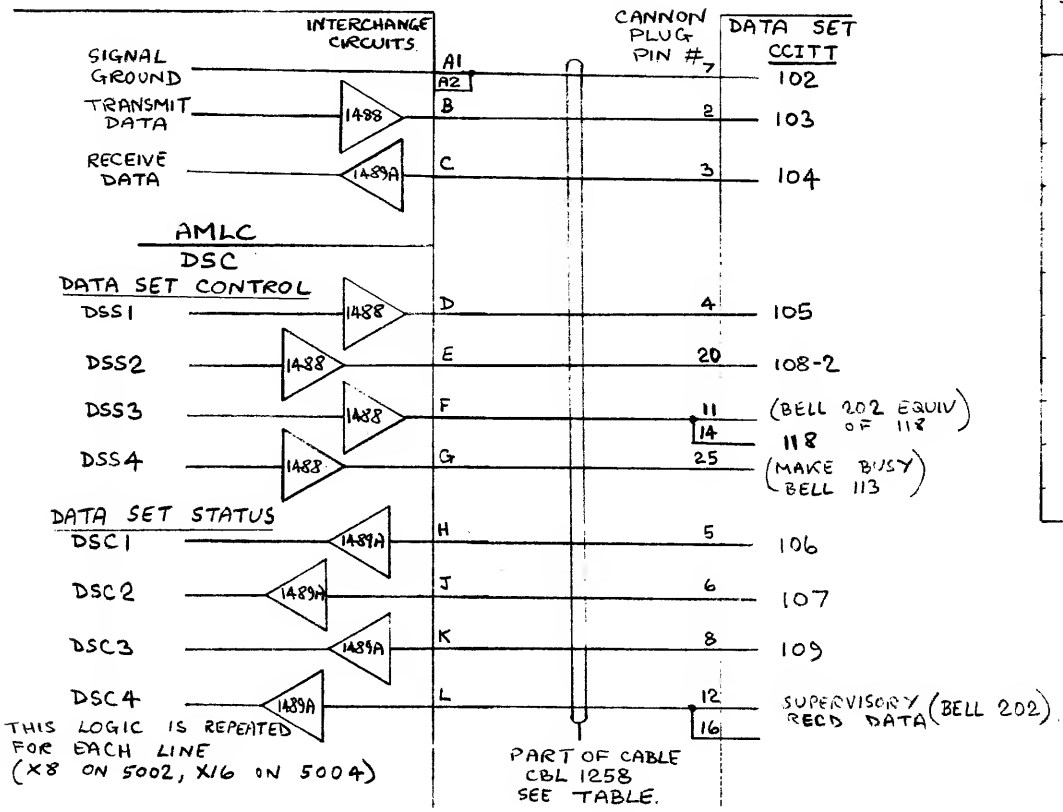
AMLC CONN PIN	LINE # / AMLC CONNECTOR & PIN #.															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	C15	C17	C11	C13	D15	D17	D11	D13	E15	E17	E11	E13	F15	F17	F11	F13
B	C9	C7	C5	C1	D9	D7	D5	D1	E9	E7	E5	E1	F9	F7	F5	F1
C	C16	C18	C12	C14	D16	D18	D12	D14	E16	E18	E12	E14	F16	F18	E12	E14
D	C33	C35	C39	C41	D33	D35	D39	D41	E33	E35	E39	E41	F33	F35	F39	F41
E	C29	C27	C25	C23	D29	D27	D25	D23	E29	E27	E25	E23	F29	F27	F25	F23

NOTE 2. FOR OTHER ASSIGNMENTS OF DATA SET STATUS (E) AND DATA SET CONTROL (B) MODIFICATIONS MUST BE MADE TO THE CABLE BY REMOVING & REASSIGNING PINS.

FIG 3 MODEL 5002, 5004 AMLC WITH CABLE CBL1258



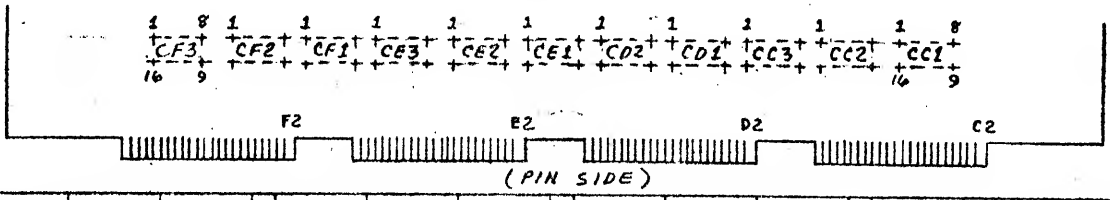
NOTE 1: MODEL 5004 IS IDENTICAL EXCEPT IT REQUIRES FOUR CABLES TO SERVICE 16 LINES



AMLC DSC CONN PIN	LINE # / AMLC CONNECTOR & PIN.																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A (1)	C16	C18	C12	C14	D16	D18	D12	D14	E16	E18	E12	E14	F16	F18	F12	F14	AMLC
A (2)	C34	C36	C40	C42	D34	D36	D40	D42	E34	E36	E40	E42	F34	F36	F40	F42	AMLC
B	C15	C17	C11	C13	D15	D17	D11	D13	E15	E17	E11	E13	F15	F17	F11	F13	AMLC
C	C33	C35	C39	C41	D33	D35	D39	D41	E33	E35	E39	E41	F33	F35	F39	F41	AMLC
D	C13	C21	C29	C37	D13	D21	D29	D37	E13	E21	E29	E37	F13	F21	F29	F37	DSC
E	C14	C22	C30	C38	D14	D22	D30	D38	E14	E22	E30	E38	F14	F22	F30	F38	DSC
F	C15	C23	C31	C39	D15	D23	D31	D39	E15	E23	E31	E39	F15	F23	F31	F39	DSC
G	C16	C24	C32	C40	D16	D24	D32	D40	E16	E24	E32	E40	F16	F24	F32	F40	DSC
H	C17	C25	C33	C41	D17	D25	D33	D41	E17	E25	E33	E41	F17	F25	F33	F41	DSC
J	C18	C26	C34	C42	D18	D26	D34	D42	E18	E26	E34	E42	F18	F26	F34	F42	DSC
K	C19	C27	C35	C43	D19	D27	D35	D43	E19	E27	E35	E43	F19	F27	F35	F43	DSC
L	C20	C28	C36	C44	D20	D28	D36	D44	E20	E28	E36	E44	F20	F28	F36	F44	DSC

NOTE 2. OTHER ASSIGNMENTS OF THE FOUR DSC/DSS LEAD BY MODIFYING THE CABLE.

LTR	DATE	REVISION	DR.	CK.



NAME	DIP SITE	CONN PIN
DSC03+	CC1-8	CC-1
GD37N	CC1-7	CC-2
DSCSA+	CC1-6	CC-3
GD18N	CC1-5	CC-4
DSC02+	CC1-9	CC-5
GD27N	CC1-10	CC-6
DSC01+	CC1-11	CC-7
GD37N	CC1-12	CC-8
DSC00+	CC1-13	CC-9
GD27N	CC1-14	CC-10
TDAT02-	CC1-15	CC-11
GD45P	CC1-16	CC-12
TDAT03-	CC2-4	CC-13
GD45P	CC2-3	CC-14
TDAT00-	CC2-2	CC-15
GD45P	CC2-1	CC-16
TDAT01-	CC2-8	CC-17
GD45P	CC2-7	CC-18
DSCSB+	CC2-6	CC-19
GD18N	CC2-5	CC-20
DSCSC+	CC2-9	CC-21
GD18N	CC2-10	CC-22
DSS23+	CC2-11	CC-23
GD41P	CC2-12	CC-24
DSS22+	CC2-13	CC-25
GD41P	CC2-14	CC-26
DSS21+	CC2-15	CC-27
GD41P	CC2-16	CC-28
DSS20+	CC2-4	CC-29
GD41P	CC2-3	CC-30
DSCSD+	CC2-2	CC-31
GD18N	CC2-1	CC-32
RDAT20-	CC3-8	CC-33
GD43P	CC3-7	CC-34
RDAT01-	CC3-6	CC-35
GD43P	CC3-5	CC-36
ADRAA-	CC3-9	CC-37
GD45L	CC3-10	CC-38
RDAT22-	CC3-11	CC-39
GD43P	CC3-12	CC-40
RDAT23-	CC3-13	CC-41
GD43P	CC3-14	CC-42
ADRAB-	CC3-15	CC-43
GD45L	CC3-16	CC-44

NAME	DIP SITE	CONN PIN
DSC07+	CC3-4	CD-1
GD27P	CC3-3	CD-2
DSCSA+	CC3-2	CD-3
GD18N	CC3-1	CD-4
DSC06+	CD1-8	CD-5
GD27P	CD1-7	CD-6
DSC05+	CD1-6	CD-7
GD27P	CD1-5	CD-8
DSC04+	CD1-9	CD-9
GD27P	CD1-10	CD-10
TDAT06-	CD1-11	CD-11
GD35P	CD1-12	CD-12
TDAT07-	CD1-13	CD-13
GD35P	CD1-14	CD-14
TDAT04-	CD1-15	CD-15
GD35P	CD1-16	CD-16
TDAT05-	CD1-4	CD-17
GD35P	CD1-3	CD-18
DSCSB+	CD1-2	CD-19
GD18N	CD1-1	CD-20
DSCSC+	CD2-8	CD-21
GD18N	CD2-7	CD-22
DSS07+	CD2-6	CD-23
GD29P	CD2-5	CD-24
DSS06+	CD2-9	CD-25
GD29P	CD2-10	CD-26
DSS05+	CD2-11	CD-27
GD29P	CD2-12	CD-28
DSS04+	CD2-13	CD-29
GD29P	CD2-14	CD-30
DSCSD+	CD2-15	CD-31
GD18N	CD2-16	CD-32
RDAT04-	CD2-4	CD-33
GD31P	CD2-3	CD-34
RDAT05-	CD2-2	CD-35
GD31P	CD2-1	CD-36
ADRAA-	CE1-8	CD-37
GD45L	CE1-7	CD-38
RDAT06-	CE1-6	CD-39
GD31P	CE1-5	CD-40
RDAT07-	CE1-9	CD-41
GD31P	CE1-10	CD-42
ADRAB-	CE1-11	CD-43
GD45L	CE1-12	CD-44

NAME	DIP SITE	CONN PIN
DSC11+	CE1-13	CE-1
GD16N	CE1-14	CE-2
DSCSA+	CE1-15	CE-3
GD18N	CE1-16	CE-4
DSC10+	CE1-4	CE-5
GD16N	CE1-3	CE-6
DSC09+	CE1-2	CE-7
GD16N	CE1-1	CE-8
DSC08+	CE2-8	CE-9
GD18N	CE2-7	CE-10
TDAT10-	CE2-6	CE-11
GD20P	CE2-5	CE-12
TDAT11-	CE2-9	CE-13
GD20P	CE2-10	CE-14
TDAT08-	CE2-11	CE-15
GD20P	CE2-12	CE-16
TDAT09-	CE2-13	CE-17
GD20P	CE2-14	CE-18
DSCSB+	CE2-15	CE-19
GD18N	CE2-16	CE-20
DSCSC+	CE2-4	CE-21
GD18N	CE2-3	CE-22
DSS11+	CE2-2	CE-23
GD16P	CE2-1	CE-24
DSS10+	CE3-8	CE-25
GD16P	CE3-7	CE-26
DSS09+	CE3-6	CE-27
GD16P	CE3-5	CE-28
DSSDB+	CE3-9	CE-29
GD16P	CE3-10	CE-30
DSCSD+	CE3-11	CE-31
GD18N	CE3-12	CE-32
RDAT24-	CE3-13	CE-33
GD18P	CE3-14	CE-34
RDAT01-	CE3-15	CE-35
GD18P	CE3-16	CE-36
ADRAA-	CE3-4	CE-37
GD45L	CE3-3	CE-38
RDAT10-	CF3-2	CE-39
GD18P	CF3-1	CE-40
RDAT11-	CF1-8	CE-41
GD18P	CF1-7	CE-42
ADRAB-	CF1-6	CE-43
GD45L	CF1-5	CE-44

NAME	DIP SITE	CONN PIN
DSC15+	CF1-9	CF-1
GD02L	CF1-10	CF-2
DSCSA+	CF1-11	CF-3
GD18N	CF1-12	CF-4
DSC14+	CF1-13	CF-5
GD02L	CF1-14	CF-6
DSC13+	CF1-15	CF-7
GD02L	CF1-16	CF-8
DSC12+	CF1-4	CF-9
GD02L	CF1-3	CF-10
TDAT14-	CF1-2	CF-11
GD10P	CF1-1	CF-12
TDAT15-	CF2-8	CF-13
GD10P	CF2-7	CF-14
TDAT12-	CF2-6	CF-15
GD10P	CF2-5	CF-16
TDAT13-	CF2-9	CF-17
GD10P	CF2-10	CF-18
DSCSB+	CF2-11	CF-19
GD18N	CF2-12	CF-20
DSCSC+	CF2-13	CF-21
GD18N	CF2-14	CF-22
DSS15+	CF2-15	CF-23
GD00P	CF2-16	CF-24
DSS14+	CF2-4	CF-25
GD00P	CF2-3	CF-26
DSS13+	CF2-2	CF-27
GD00P	CF2-1	CF-28
DSS12+	CF3-8	CF-29
GD06P	CF3-7	CF-30
DSCSD+	CF3-6	CF-31
GD18N	CF3-5	CF-32
RDAT12-	CF3-8	CF-33
GD08P	CF3-10	CF-34
RDAT13-	CF3-11	CF-35
GD08P	CF3-12	CF-36
ADRAA-	CF3-13	CF-37
GD45L	CF3-14	CF-38
RDAT14-	CF3-15	CF-39
GD16P	CF3-16	CF-40
RDAT15-	CF3-4	CF-41
GD08P	CF3-3	CF-42
ADRAB-	CF3-2	CF-43
GD45L	CF3-1	CF-44

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	AMLC CONNECTOR SIGNAL NAME LIST
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF 3 — SIZE C — DWG. NO. LBD 1208 — REV. B